34980A System Control Modules

34950A 64-bit digital I/O with memory and counter

This module can be used to simulate or detect digital patterns. It has eight 8-bit digital I/O channels with handshaking, pattern memory, two 10 MHz counters with gate functions, and a programmable clock output.

Digital input/output

The digital I/O bits are organized into two banks of 32-bits. The I/O bits can be configured and programmed as inputs or outputs in 8-bit channels. The digital outputs can be configured as active drive or open drain outputs with a 10 kΩ pull up. User supplied pull up resistors for up to 5 V outputs are also acceptable. The digital inputs have programmable thresholds up to 5 V for compatibility with most digital logic standards.

The onboard pattern memory can be used to select and output digital stimulus or bitstream patterns, or to capture external digital data. Each bank has independent memory and directional control so that one bank can output data while the other captures data. The memory can be divided up to 64 Kbytes per 8-bit channel.

Specifically, the digital I/O channels also have:
- Variable active high drive output from 1.65 V to 5 V or open drain
- Variable input thresholds from 0 V to 5 V
- Configurable handshaking protocols including synchronous, and strobe
- Programmable polarity
- Source or sink up to 24 mA with a I_{max} of 400 mA per module.
- Internal alarming for maskable pattern match
- 1 hardware pattern interrupt per bank
- Connections via standard 78-pin Dsub cables or detachable terminal block

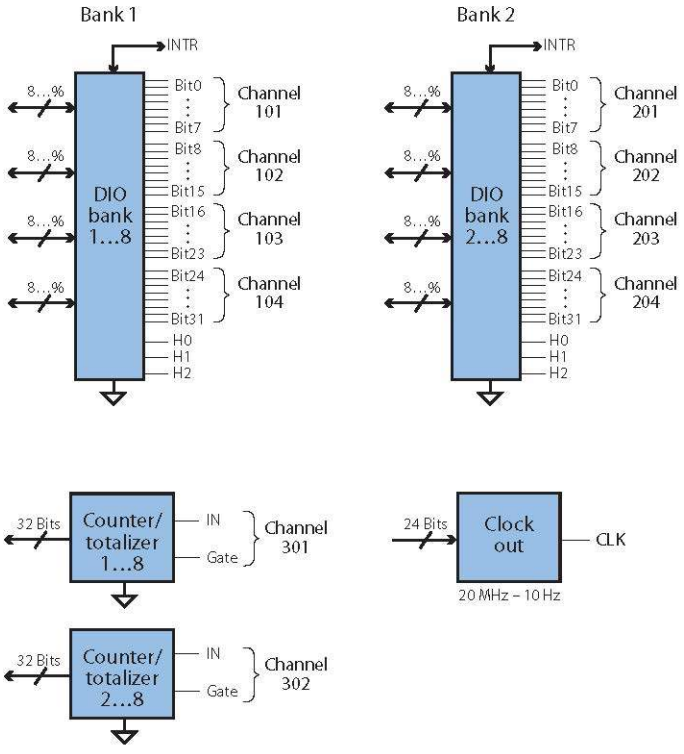

Figure 13. 34950A 64-channel digital I/O

Frequency counter/totalizer

The two channels can be used to count digital events, frequency, period, duty cycle, totalize, and pulse width. The counter/ totalizer also includes
- Programmable gate functionality
- Programmable input thresholds levels 0 V to 3 V

Digital input/output characteristics	
Eight 8-bit channels: 8 bits wide, input or output, non-isolated	
Vin	0 V – 5 V [1]
Vout	1.65 V – 5V [1, 2]
Iout	(max) 24 mA [2]
Frequency (max)	10 MHz [3]
I_{Load} (max)	400 mA
$t_{rise} + t_{fall}$ (typ)	6 ns [5]
Handshake lines	
Vin	0 – 5 V [4]
Vout	1.65 – 5 V [2, 4]
I out (max)	24 mA [2]
Frequency (max)	10 MHz
Counter function characteristics	
Max freq	10 MHz (max) 50% duty cycle
Vin	0 V – 5 V
Min rise/fall time	5 µsec
Totalizer function characteristics	
Maximum count	2^32 – 1 (4,294,967,296)
Max input freq	10 MHz (max), rising or falling edge programmable
Vin	0 V – 5 V
Gate input	0 V – 5 V
Min rise/fall time	5usec
System clock generator characteristics	
Frequency	20 MHz – 10 Hz configurable divideby-n 24-bits, programmable on/off
Vout	1.65 V – 5 V [2]
I out (max)	24 mA [2]
Accuracy:	100 ppm

[1] Configurable by 8-bit channel
[2] Lower current drive at lower voltages
[3] From memory with handshaking
[4] Configurable by bank
[5] 5 V, 50 pF load